July 2008

FAIRCHILD SEMICONDUCTOR®

FDW2521C

Complementary PowerTrench® MOSFET

General Description

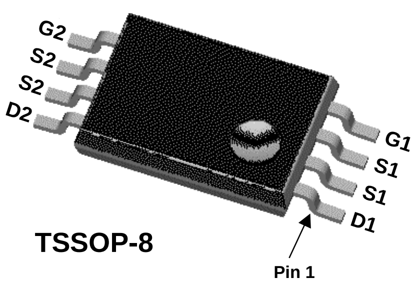
This complementary MOSFET device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

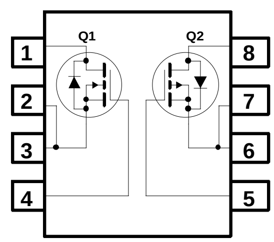
Applications

- DC/DC conversion
- Power management
- Load switch

Features

- **Q1: N-Channel**
  5.5 A, 20 V. $R_{DS(ON)}$ = 21 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 35 mΩ @ V_{GS} = 2.5 V
- **Q2: P-Channel**
  –3.8 A, 20 V. $R_{DS(ON)}$ = 43 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 70 mΩ @ V_{GS} = –2.5 V
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		20	–20	V
V_{GSS}	Gate-Source Voltage		±12	±12	V
I_D	Drain Current - Continuous	(Note 1a)	5.5	–3.8	A
	- Pulsed		30	–30	
P_D	Power Dissipation	(Note 1a)	1.0		W
		(Note 1b)	0.6		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	125	°C/W
		(Note 1b)	208	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2521C	FDW2521C	13''	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA V_{GS} = 0 V, I_D = –250 µA	Q1 Q2	20 –20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = –250 µA, Referenced to 25°C	Q1 Q2		14 –16		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V V_{DS} = –16 V, V_{GS} = 0 V	Q1 Q2			1 –1	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V V_{GS} = ±12 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA V_{DS} = V_{GS}, I_D = –250 µA	Q1 Q2	0.6 –0.6	0.8 –1.0	1.5 –1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = –250 µA, Referenced to 25°C	Q1 Q2		–3.2 3.0		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 5.5 A V_{GS} = 2.5 V, I_D = 4.2 A V_{GS} = 4.5 V, I_D = 5.5 A, T_J = 125°C	Q1		17 24 23	21 35 34	mΩ
		V_{GS} = –4.5 V, I_D = –3.8 A V_{GS} = –2.5 V, I_D = –3.0 A V_{GS} = –4.5 V, I_D = –3.8 A, T_J = 125°C	Q2		36 56 49	43 70 69	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V V_{GS} = –4.5 V, V_{DS} = –5 V	Q1 Q2	30 –15			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 5.5 A V_{DS} = –5 V, I_D = –3.5 A	Q1 Q2		26 13.2		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz Q2: V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		1082 1030		pF
C_{oss}	Output Capacitance		Q1 Q2		277 280		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		130 120		pF
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω Q2: V_{DD} = –5 V, I_D = –1 A, V_{GS} = –4.5V, R_{GEN} = 6 Ω	Q1 Q2		8 11	20 20	ns
t_r	Turn-On Rise Time		Q1 Q2		8 18	27 32	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		24 34	38 55	ns
t_f	Turn-Off Fall Time		Q1 Q2		8 34	16 55	ns
Q_g	Total Gate Charge	Q1: V_{DS} = 10 V, I_D = 5.5 A, V_{GS} = 4.5 V Q2: V_{DS} = –5 V, I_D = –3.8 A, V_{GS} = –4.5 V	Q1 Q2		12 9.7	17 16	nC
Q_{gs}	Gate-Source Charge		Q1 Q2		2 2.2		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		3 2.4		nC

Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			0.83 –0.83	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.83 A (Note 2) V_{GS} = 0 V, I_S = –0.83 A (Note 2)	Q1 Q2		0.7 –0.7	1.2 –1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ is 125°C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.

b) $R_{\theta JA}$ is 208°C/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics: Q1

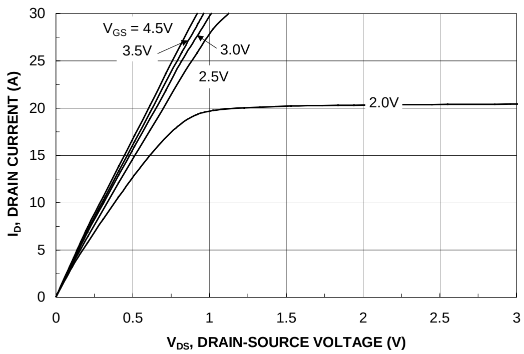


Figure 1. On-Region Characteristics.

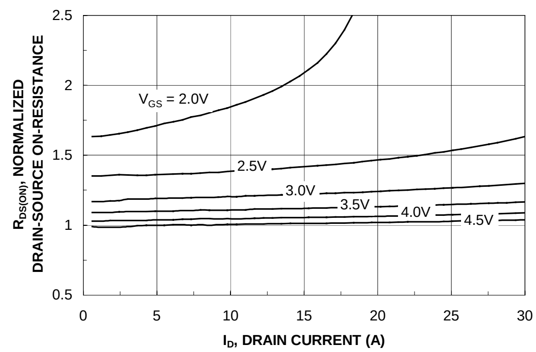


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

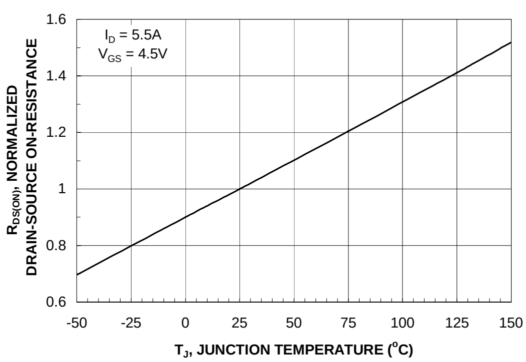


Figure 3. On-Resistance Variation with Temperature.

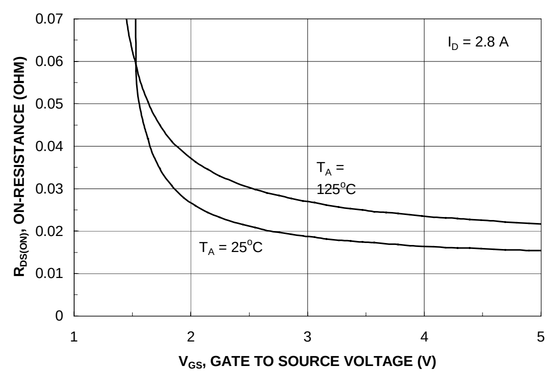


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

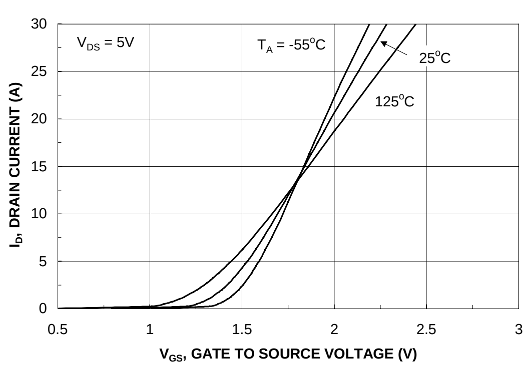


Figure 5. Transfer Characteristics.

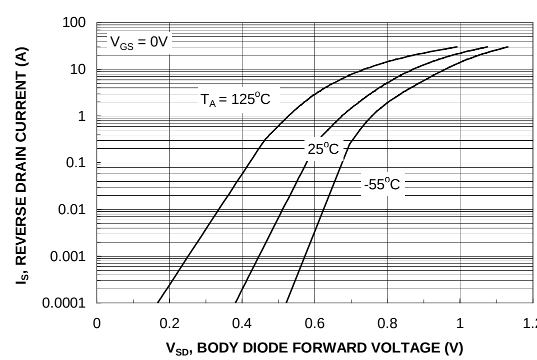


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1

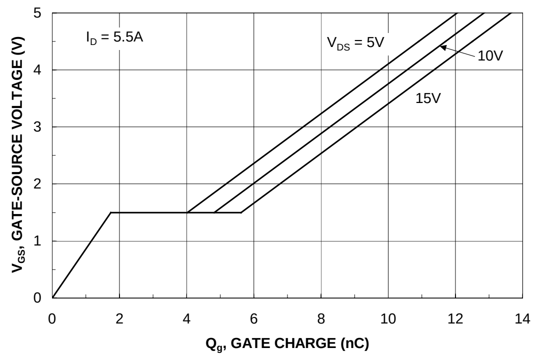


Figure 7. Gate Charge Characteristics.

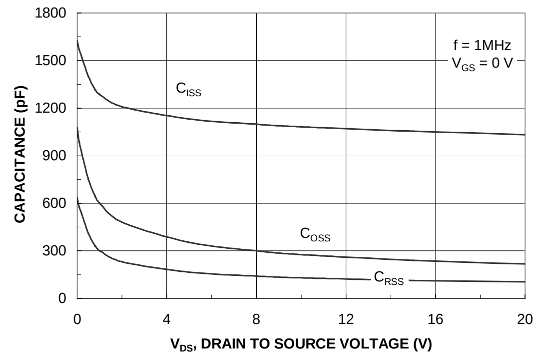


Figure 8. Capacitance Characteristics.

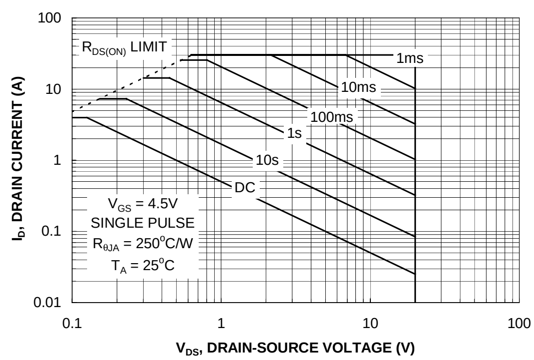


Figure 9. Maximum Safe Operating Area.

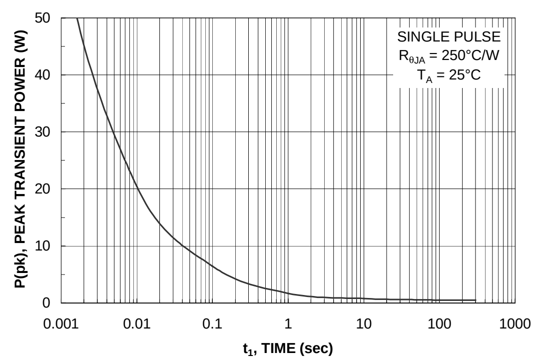


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q2

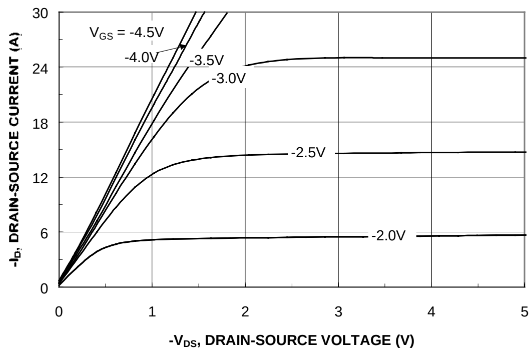


Figure 11. On-Region Characteristics.

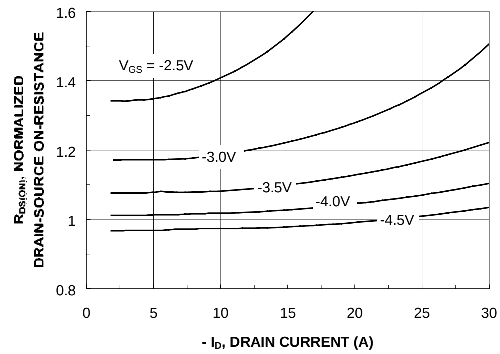


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

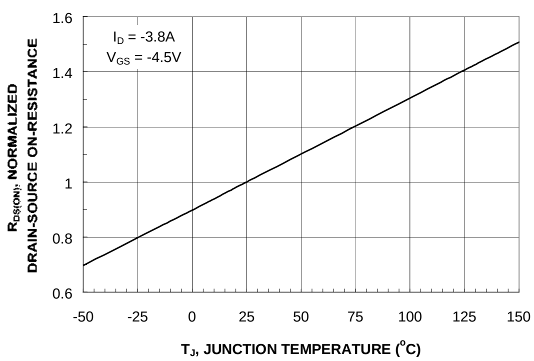


Figure 13. On-Resistance Variation with Temperature.

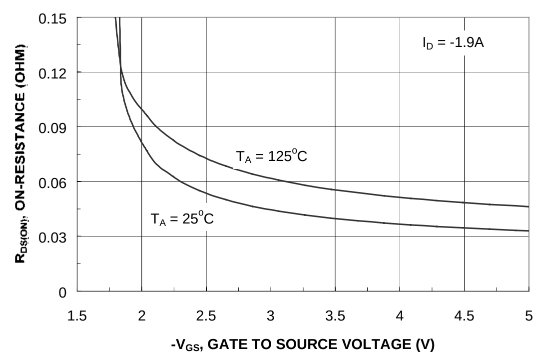


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

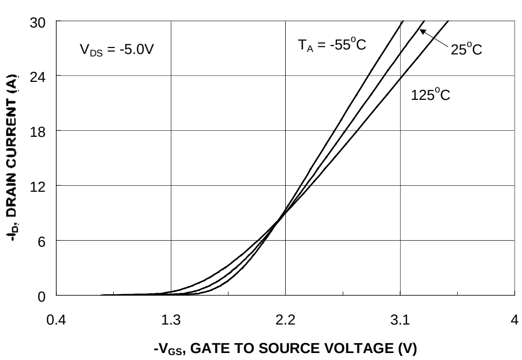


Figure 15. Transfer Characteristics.

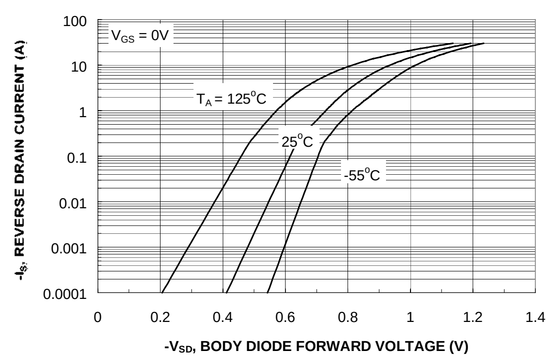


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

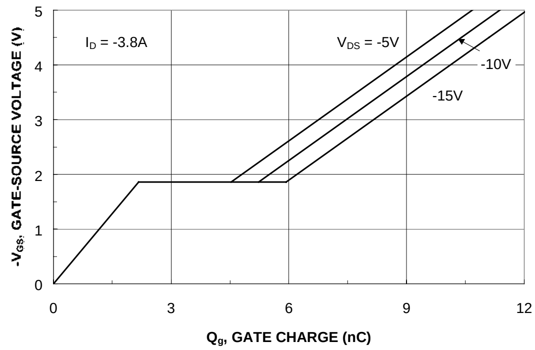


Figure 17. Gate Charge Characteristics.

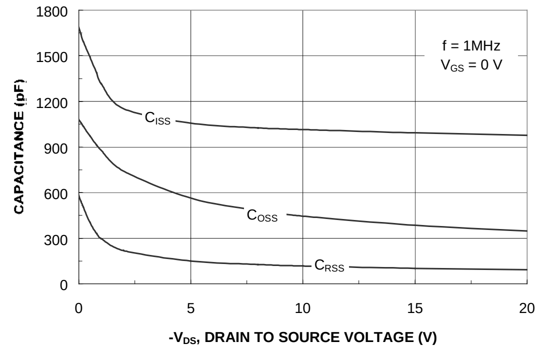


Figure 18. Capacitance Characteristics.

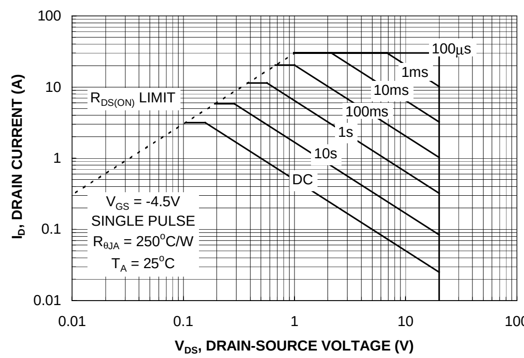


Figure 19. Maximum Safe Operating Area.

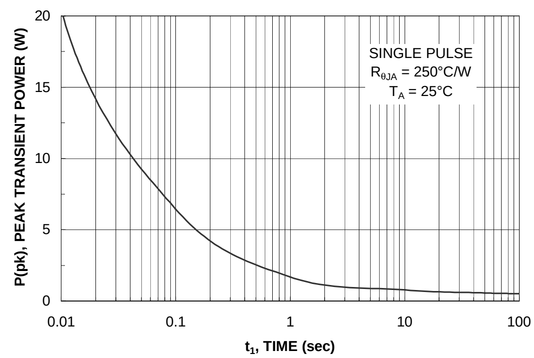


Figure 20. Single Pulse Maximum Power Dissipation.

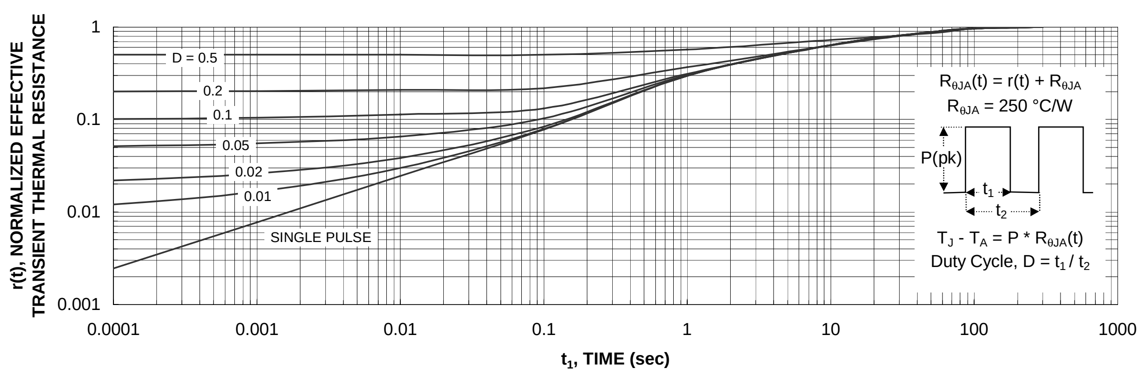


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidianries, and is not intended to be an exhaustive list of all such trademarks.

Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EfficentMax™
EZSWITCH™ *
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter® *
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
PDP SPM™
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW at a time™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SuperMOS™
SyncFET™
The Power Franchise®
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Farichild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Farichild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Farichild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Farichild is committed to committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I35